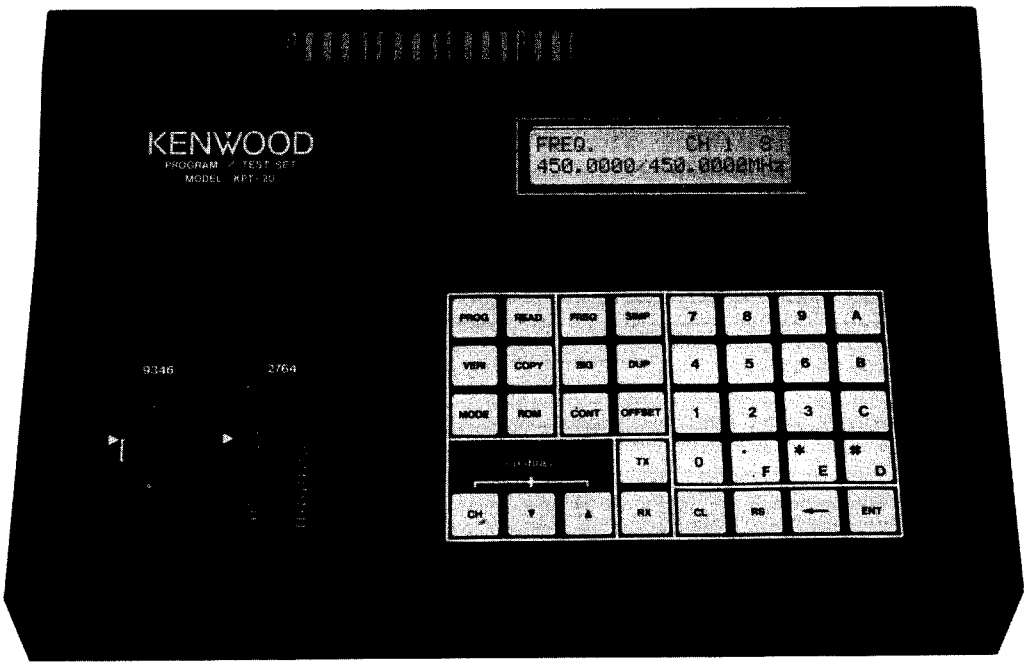
PROGRAM/TEST SET

KPT-20

SERVICE MANUAL

KENWOOD

B51-3158-00 (O) 1844



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CIRCUIT DESCRIPTION

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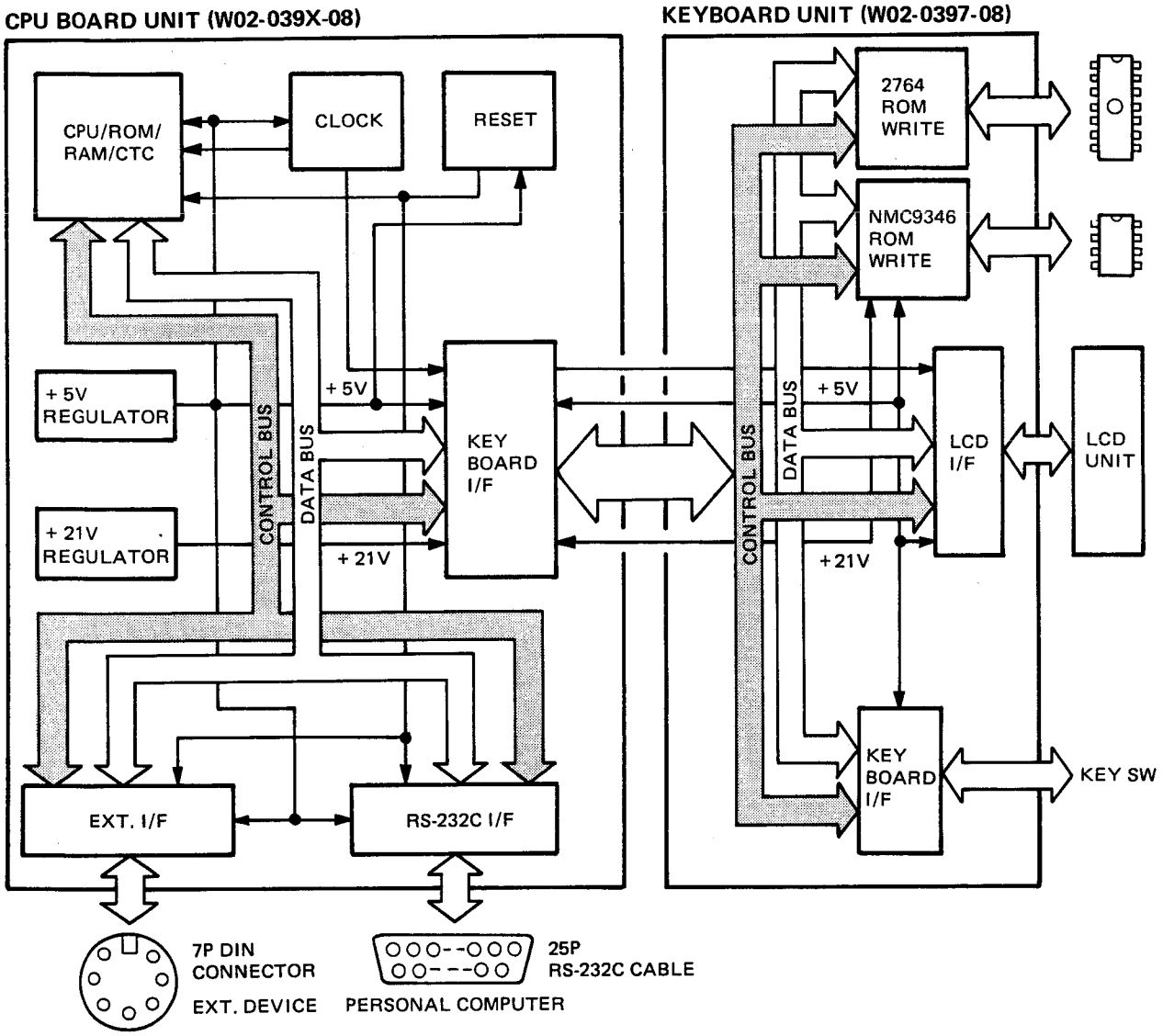


Fig. 1 KPT-20 Block Diagram

CPU Board Unit

The CPU board un t is a microcomputer consisting of a microprocessor CPU, ROM, RAM, CTC, parallel I/O interface to the keyboard unit, RS-232C interface, external interface, +5V and +21V power supplies, clock, and reset circuit.

Keyboard Unit

The keyboard unit consists of a ROM writer, keyboard, LCD controller, 2764 ROM write section, NMC9346 ROM write section, LCD interface, and keyboard interface.

CIRCUIT DESCRIPTION

CPU, ROM, RAM and CTC Circuits

The microprocessor (CPU) uses SN74LS139N (IC18) to decode memory addresses and SN74LS139N (IC12) to decode I/O addresses. A memory address map and I/O address map are shown below.

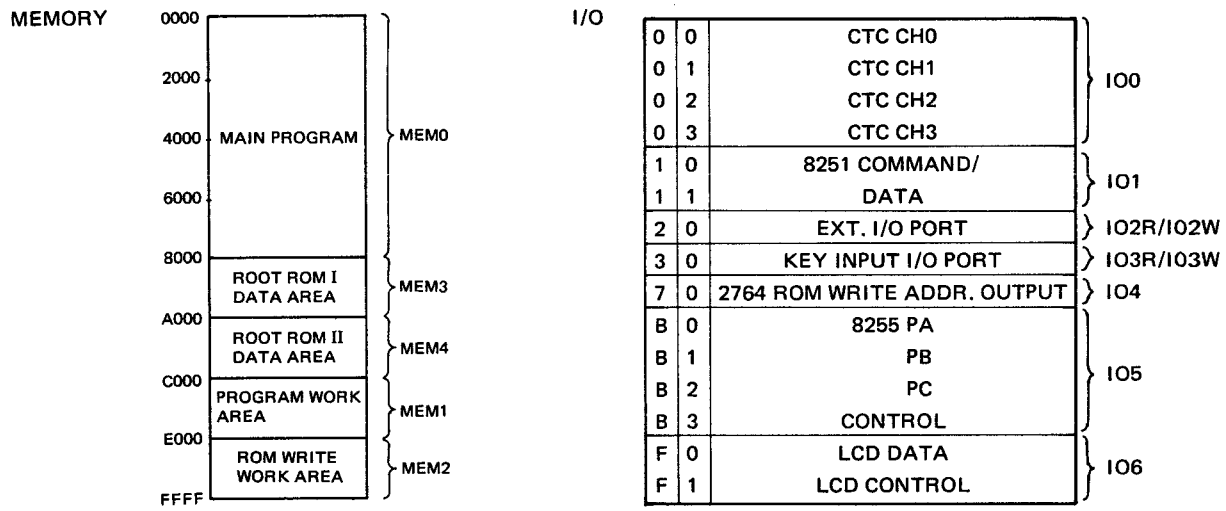


Fig. 2 Memory Address Map and I/O Address Map

Address Bus

The address lines A0 to A15 of the microprocessor LH0080A (IC25) are distributed as follows: A13 to A15 to the memory address decoder IC18; A4 to A7 to the I/O address decoder IC12; A0 and A1 to the timer LH0082A (IC24); A0 to A12 to the root ROM (IC13, IC19); A0 to A12 to the RAM MB846415L (IC8 and IC14); A0 to A13 to the ROM MBM27256 (IC20); A0 to the RS-232C interface μPD8251AP-5 (IC5); and A0 and A1 to the interface buffer SN74LS244N (IC9) with the keyboard unit.

INPUTS			OUTPUTS			
ENABLE	SELECT					
1G	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

1A = $\overline{\text{RFSH}}$
1B = A15
1G = $\overline{\text{MREQ}}$

1Y1 = $\overline{\text{MEMO}}$ (IC20)
1Y3 = 2G

INPUTS			OUTPUTS			
ENABLE	SELECT					
2G	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

2A = A13
2B = A14
2G = 1Y3 (IC18)

2Y0 = $\overline{\text{MEM3}}$ (IC19)
2Y1 = $\overline{\text{MEM4}}$ (IC13)
2Y2 = $\overline{\text{MEM1}}$ (IC14)
2Y3 = $\overline{\text{MEM2}}$ (IC8)

Table 1 IC18 (Memory Address Control)

INPUTS			OUTPUTS			
ENABLE	SELECT					
1G	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

1A = A6
1B = A7
1G = 2Y3 (IC12)

1Y0 = IC11
1Y1 = IC11
1Y2 = IO5 (IC15)
1Y3 = IO6 (IC15)

INPUTS			OUTPUTS			
ENABLE	SELECT					
2G	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

2A = A4
2B = A5

2Y0 = IO0 (IC24)
2Y1 = IO1 (IC5)
2Y2 = IC10
2Y3 = IC10

Table 2 IC12 (I/O Address Control)

CIRCUIT DESCRIPTION

Data Bus

The data lines D0 to D7 of the microprocessor (IC25) act as input lines when $\overline{RD}$ is "L" and as output lines when $\overline{WR}$ is "L". These lines are connected to the peripheral I/O circuits (IC4, IC5, IC9, IC21, IC24) of the memory IC (IC8, IC13, IC14, IC19, IC20).

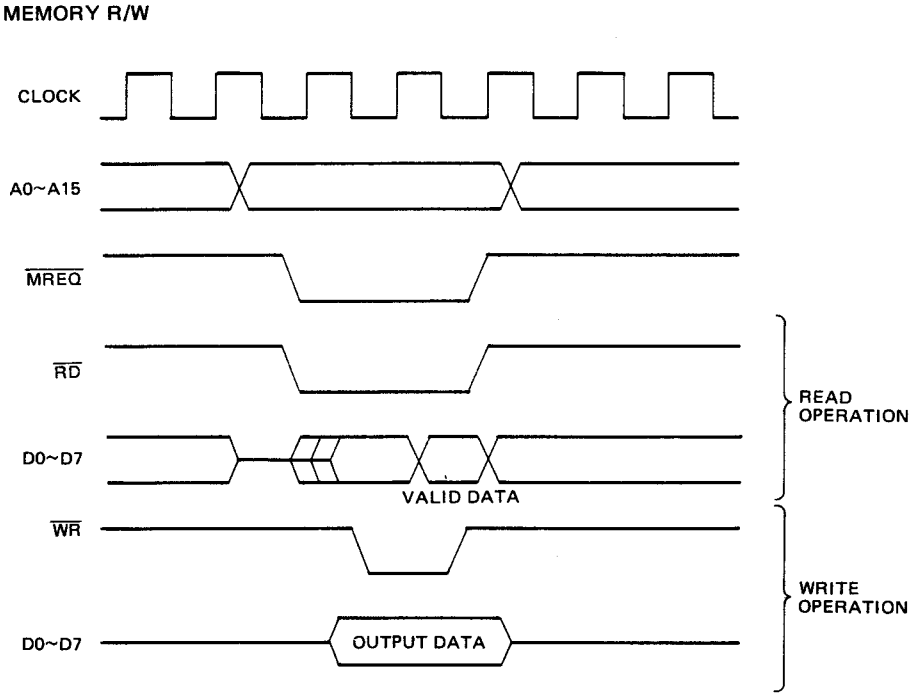


Fig. 3 Memory Read/Write Operation Timing Chart

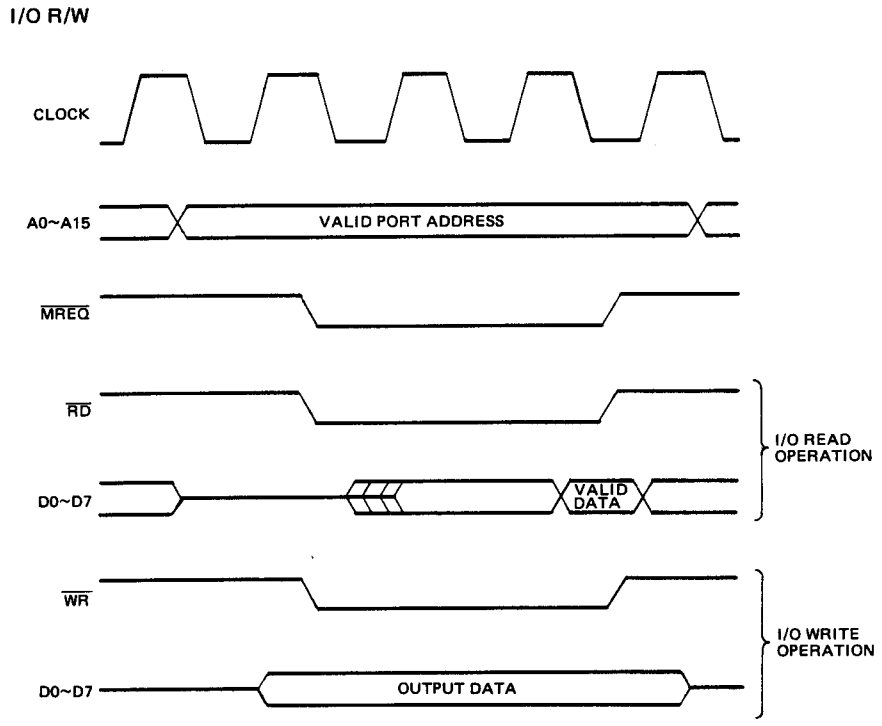


Fig. 4 I/O Read/Write Operation Timing Chart

CIRCUIT DESCRIPTION

Keyboard Unit Interface Circuit

The keyboard unit interface consists of the three-state bus buffers SN74LS245N (IC21, IC9), and SN74LS244N (IC15) shown in **Fig. 5**. This circuit interfaces the bi-directional data bus to the keyboard unit, various circuit control lines, and the power lines. IC21 is a three-state bidirectional bus transceiver that interfaces the bus lines to the keyboard unit. Its operation is controlled by pin 19 ($\overline{G}$) as follows:

When the I/O address is 30H, 70H, B0H, B1H, B2H, B3H, F0H or F1H and the $\overline{IORQ}$ output from the microprocessor is "L", $\overline{GATE}$ (which is the $\overline{G}$ input of IC21) goes "L". For an I/O access on the CPU board, $\overline{GATE} = \overline{G}$ is always "H", placing IC21 in the high-impedance state. For a keyboard unit I/O access $\overline{GATE} = \overline{G}$ is always "L" and IC21 is connected to the bus.

The bus direction is controlled by pin 1 (DIR) of IC21 as follows:

The $\overline{IORQ}$ and $\overline{RD}$ outputs from the microprocessor to SN74LS32N (IC10) generate the $\overline{IOR}$ signal, which is input to pin 1 (DIR) of IC21. In an I/O read operation, $\overline{IOR}$ = DIR is "L". In a write operation from the keyboard unit to the CPU board unit $\overline{IOR}$ = DIR is "H".

This signal switches the bus direction between the CPU board unit and the keyboard unit.

Bus direction	$\overline{G}$	DIR
KEY BOARD → CPU BOARD	L	L
KEY BOARD ← CPU BOARD	L	H
KEY BOARD X CPU BOARD	H	H/L

X : No direction

Table 3 Bus Direction between Keyboard Unit and CPU Board Unit

IC9 is a three-state bus buffer that interfaces four bus lines to the keyboard unit which are used as a 4-bit read port. The $\overline{IO2R}$ signal generated by SN74LS139N (IC12) and SN74LS244N (IC11) is input at pin 19 of IC9. The bus is connected only when $\overline{IO2R} = \overline{2G}$ is "L".

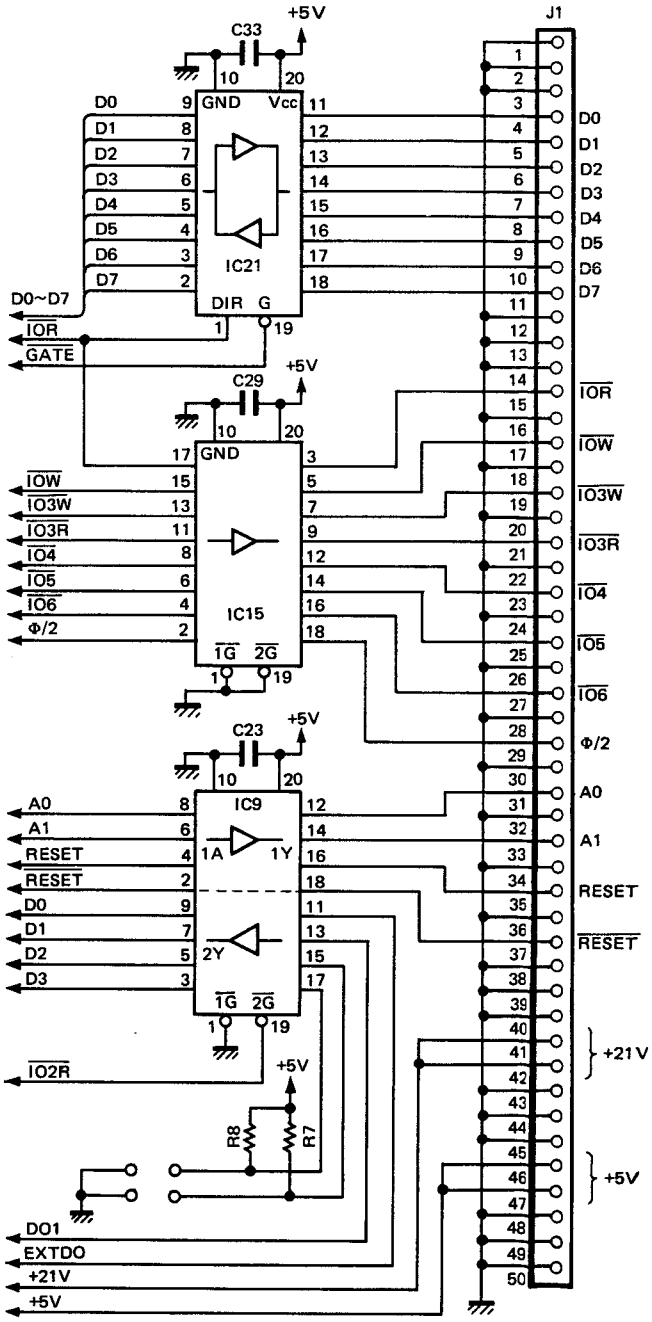


Fig. 5 Keyboard Unit Interface Circuit Block Diagram

CIRCUIT DESCRIPTION

RS-232C Interface Circuit

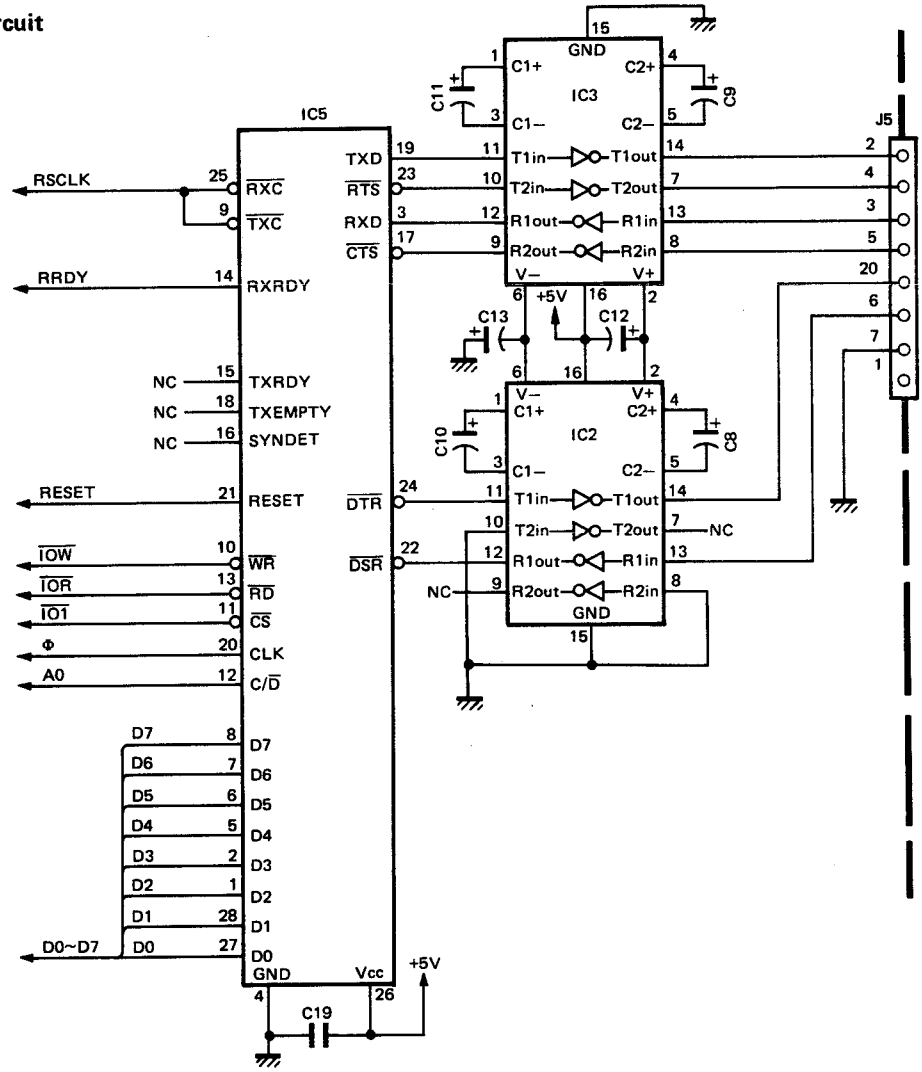


Fig. 6 RS-232C Interface Circuit Block Diagram

The RS-232C interface circuit consists of μPD8251AP-5 (IC5), MAX232 (IC2 and IC3) as shown in **Fig. 6.** This circuit performs RS-232C input and output using the standard 8251 IC. The transmitter and receiver ICs are MAX232 that generate ±10V signals from + 5V inputs.

The MAX232 has two internal charge pump circuits. One of these uses an external capacitor (C11) to create + 10V output from + 5V input; the other uses capacitor C9 to create −10V output from + 10V input. Pins 25 and 9 of IC5 input the clock signals that control the rate at which characters are sent and received.

The clock signals are generated by IC24. Pin 10 inputs the $\overline{IOW}$ signal generated by IC10 from the $\overline{WR}$ and $\overline{IORQ}$ outputs from the microprocessor. Pin 13 inputs the $\overline{IOR}$ signal created by IC10 from the $\overline{RD}$ and $\overline{IORQ}$ outputs from the microprocessor. Pin 11 inputs the decoded signal from pin 11 of IC12. Pin 12 inputs A0 from the microprocessor's address bus.

12 pin C/$\overline{D}$	13 pin $\overline{RD}$	10 pin $\overline{WR}$	11 pin $\overline{CS}$	Function
0	0	1	0	μPD8251AF data → Data bus
0	1	0	0	Data bus → μPD8251AF data
1	0	1	0	Status → Data bus
1	1	0	0	Data bus → Control
X	1	1	0	Data bus → Hi-Z
X	X	X	1	Data bus → Hi-Z

Table 4 IC5 Pin Function

CIRCUIT DESCRIPTION

External Interface Circuit

The external interface circuit consists of SN74LS237N (IC4) and SN74LS244N (IC1) as shown in **Fig. 7**. This circuit is an interface for reading and writing an external ROM (NMC9346). It also includes a circuit for reading the NMC9346 root ROM. IC4 switches the gate (IC1) of the three-state buffer of the external signal lines on and off, and controls the SK, CS, DI, and external Reset signals of the NMC9346. SK and DI are for both the root ROM and external ROM. Pins 1 and 19 of IC1 are "H" when the external ROM is not accessed, in which case the outputs of IC1 are in the high-impedance state. The timing of EXTSK, EXTD1, EXTCS, and EXTDO is as shown in the timing chart of the NMC9346 ROM write circuit.

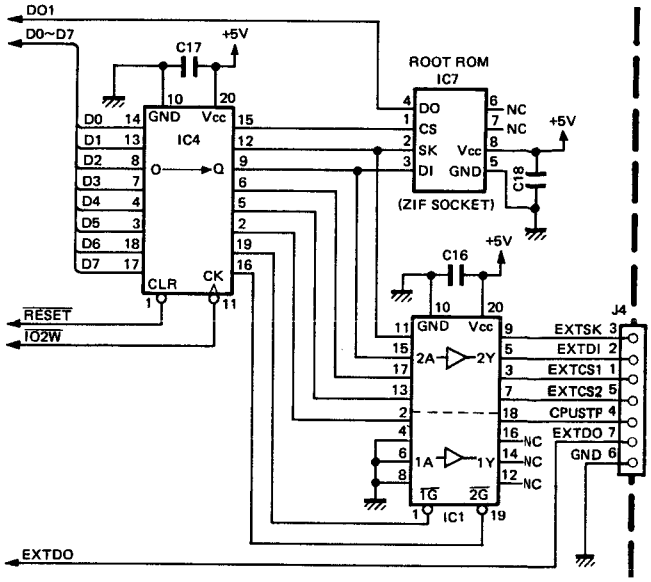


Fig. 7 External Interface Circuit Block Diagram

+ 5V Power Supply Circuit

The + 5V power supply circuit consists of a three-pin regulator L7805 (IC26) and two 2SA1265 power transistors (Q1 and Q2), forming a series power supply. This circuit supplied + 5V power to all IC etc. in the device. It is designed for a maximum output current of 2A. Q1 and Q2 are used for current boosting.

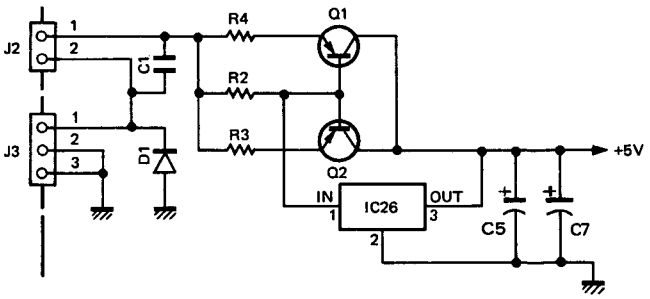


Fig. 8 + 5V Power Supply Circuit Block Diagram

+ 21V Power Supply Circuit

The + 21V power supply circuit consists of a switching regulator TL497AC (IC6) with an external coil, capacitor, and resistors as shown in **Fig. 9**. This power supply circuit generates the + 21V Vpp used for ROM writing. The + 21V voltage is determined by the R5—R6 voltage divider. R5 and R6 are accordingly metal-film precision resistors. The theoretical output voltage is given by the following formula:

$V_O = 1.2V \times (20k\Omega + 1.2k\Omega)/1.2k\Omega = 21.2V$

The 1.2V in this formula is the comparator reference voltage of IC6. C4 is a 100pF timing capacitor that controls the ON time of the oscillator, giving an ON time of 11μs. R1 is a current limiting resistor. Switching stops if the peak current flowing through R1 exceeds 500mA. Excessive current is detected as the voltage difference between pins 13 and 14 of IC6. Pin 10 of IC6 is the collector of the internal transistor while pin 8 is the emitter. The transistor turns on only for the ON time determined by C4. While this transistor is on, electromagnetic energy is stored in coil L1, to be added to the voltage from the power supply when the transistor is off.

Pin 7 of IC6 is the anode of the internal Schottky barrier diode, while pin 6 is the cathode. This diode prevents flow of charge to C2 while the internal transistor is on.

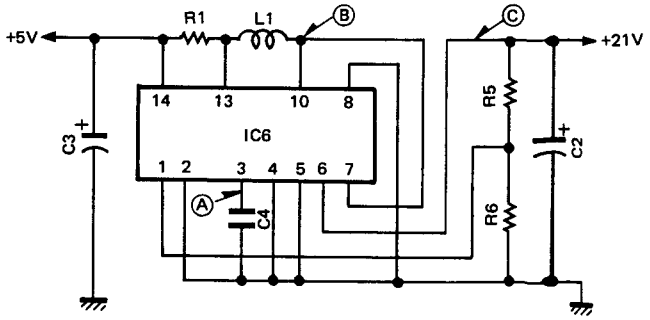


Fig. 9 + 21V Power Supply Circuit Block Diagram

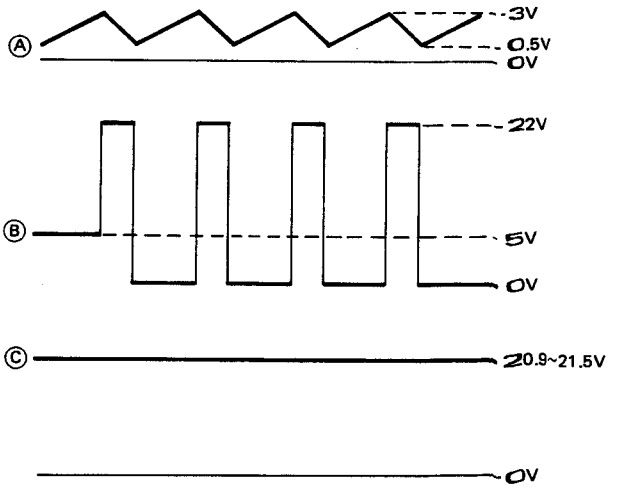


Fig. 10 + 21V Power Supply Circuit Timing Chart

CIRCUIT DESCRIPTION

Clock Circuit

The clock circuit consists of a crystal oscillator (X1), a SN74LS04A (IC23) and a SN74LS74N (IC22) as shown in **Fig. 11**. The LH0080A microprocessor operates on the 2.4576MHz system clock. This clock output is also connected to the CTC and used as the baud rate generator of the RS-232C input/output IC μPD8251AC-5. IC22 divides the frequency in half to provide a 1.2288MHz clock for the LCD ass'y.

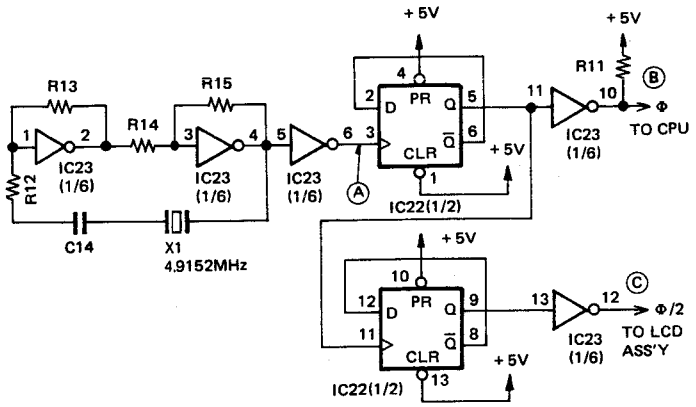


Fig. 11 Clock Circuit Block Diagram

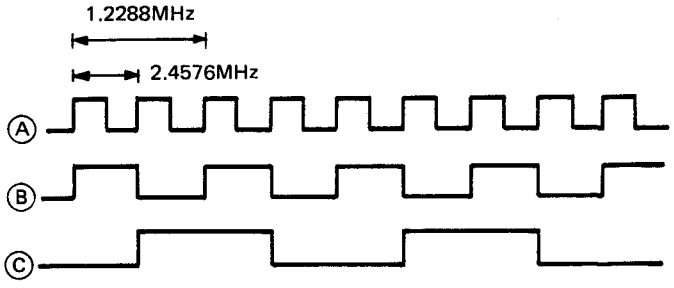


Fig. 12 Clock Circuit Timing Chart

Reset Circuit

The reset circuit consists of a reset IC PST520C (IC16), resistors and a capacitor that determine the reset time constant (R9, R10, and C15), and a Schumitt trigger inverter SN74LS14 (IC17). When the supply voltage falls to 4.5V, the reset IC (IC16) sends a Reset signal to the microprocessor and I/O devices, halting execution. When the supply voltage becomes higher than 4.5V the Reset signal is cleared. After a waiting time determined by the R10–C15 time constant the microprocessor is initialized and starts running.

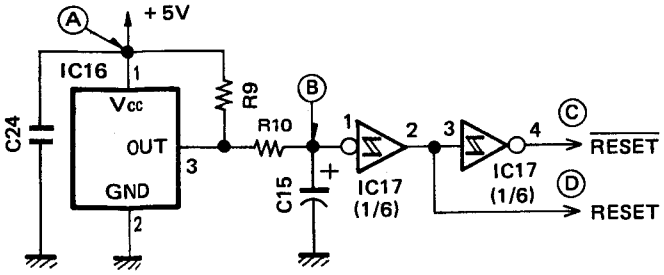


Fig. 13 Reset Circuit Block Diagram

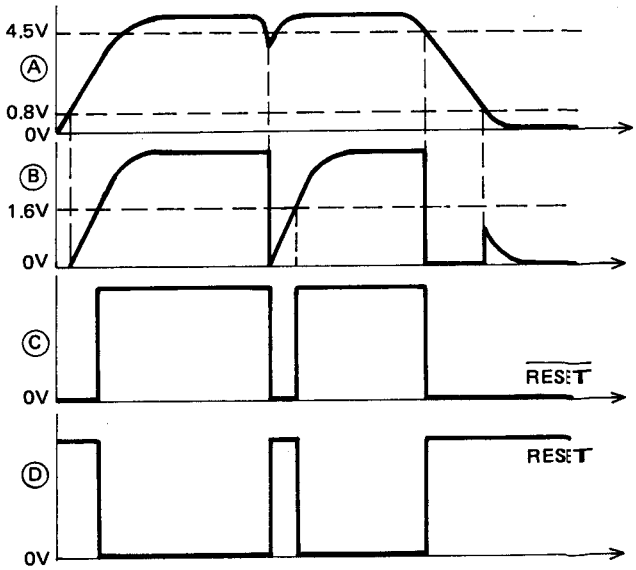


Fig. 14 Reset Circuit Timing Chart

CIRCUIT DESCRIPTION

2764 ROM Write Circuit

In the 2764 ROM write circuit, PB of μPD8255AC-5 (IC2) is assigned to the 2764 data bus, while PA and bit 5 of IC7 are assigned to the address bus. Transistors Q5 and Q6 are used to detect reverse insertion of the ROM. If the ROM is inserted backward, current flows from pin 28 to pin 14 of the Zero insertion force (ZIF) socket, dropping the base voltage of Q6, causing "H" input to be detected at pin 17 of IC5. When the ROM is not inserted backward "L" input is detected. Transistor Q4 is switched to provide + 5V to Vcc; transistor Q8 is switched to provide + 5V to Vpp; transistor Q7 is switched to provide + 21V to Vpp.

The $\overline{OE}$, $\overline{CE}$, and $\overline{PGM}$ lines of the ROM are assigned to IC7. All the ROM pins are under software control.

IC7 is a high-voltage buffer used to protect IC2 and IC4.

Q9 operates as an inverter.

Q5, R11, R29, and R28 form a constant-current circuit.

D2 protects Q5.

Q4 performs + 5V switching for Vcc. (VCE $\leqq$ −0.3V)

Q7 performs + 21V switching for Vpp. (VCE $\leqq$ −0.3V)

Q8 performs + 5V switching for Vpp. (VCE $\leqq$ −0.3V)

D3 protects Q8 when + 21V is on.

D3 is a Schottky barrier diode that reduces the voltage drop when the + 5V supply is on. The voltage drop is + 0.5V or less at D3 and Q8. When Q7 is on, Vpp is + 20.9V to + 21.5V.

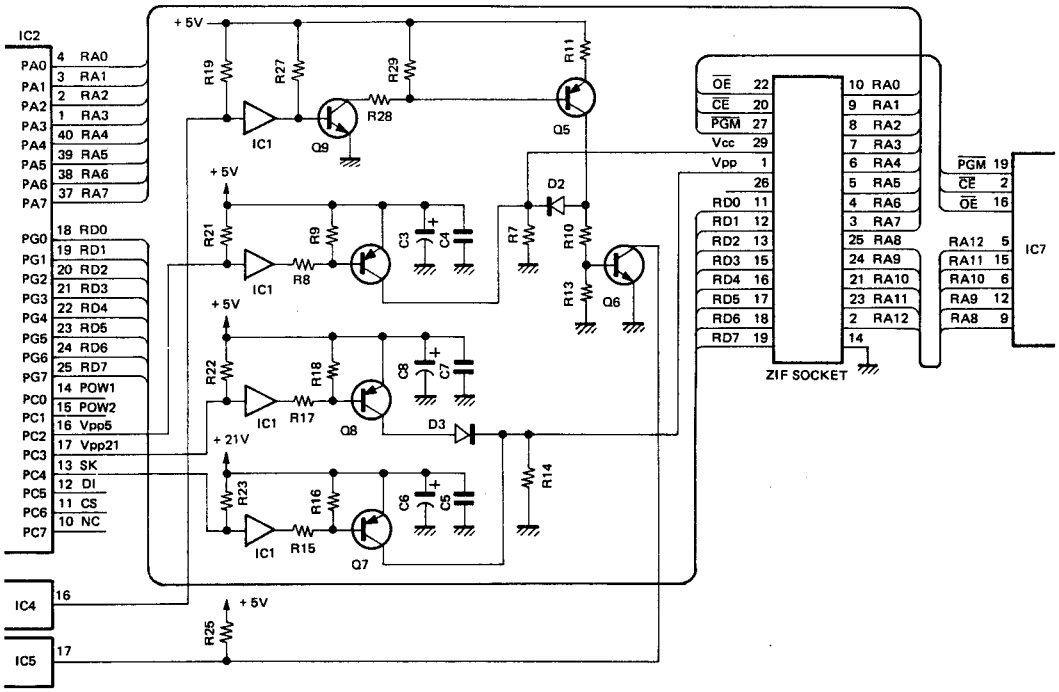


Fig. 15 2764 ROM Write Circuit Block Diagram

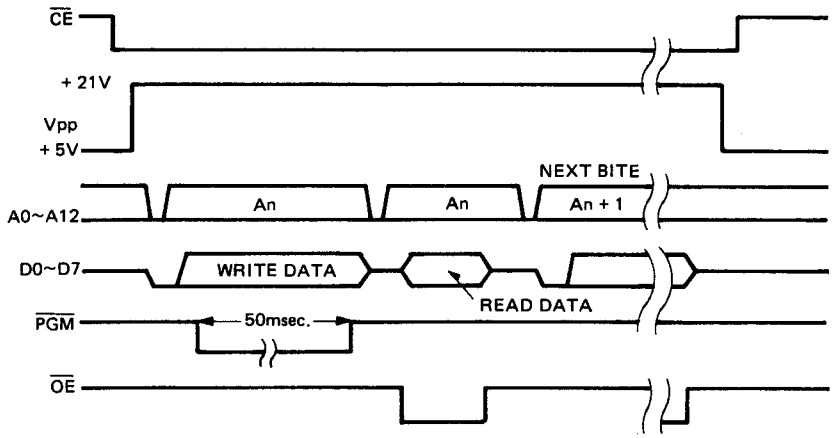


Fig. 16 2764 ROM Write Circuit Timing Chart

CIRCUIT DESCRIPTION

NMC9346 ROM Write Circuit

In the NMC9346 ROM write circuit, PC of μPD8255AC-5 (IC2) is assigned to SK, DI, and CS of the NMC9346. Q3 is switched for Vcc of the NMC9346. Q1 and Q2 are used to detect reverse insertion of the ROM. Reverse insertion is detected by normally feeding a "H" output from pin 15 of IC4 to pin 8 of IC5. When the ROM is inserted backward, the base potential of Q2 drops and "L" input is detected at pin 8 of IC5.

Transistors Q1 and Q2 are used to test for reverse insertion. If the ROM is inserted backward, pins 1 and 5 are interchanged; that is, CS and GND are interchanged. The current across this interval is sensed by Q2. When pin 5 of IC1 is "H", the emitter voltage of Q2 is approximately + 2.2V. When base current is present current also flows to the base of Q1, which turns on, at which point reverse insertion is detected by software. D1 is a protection diode for Q2.

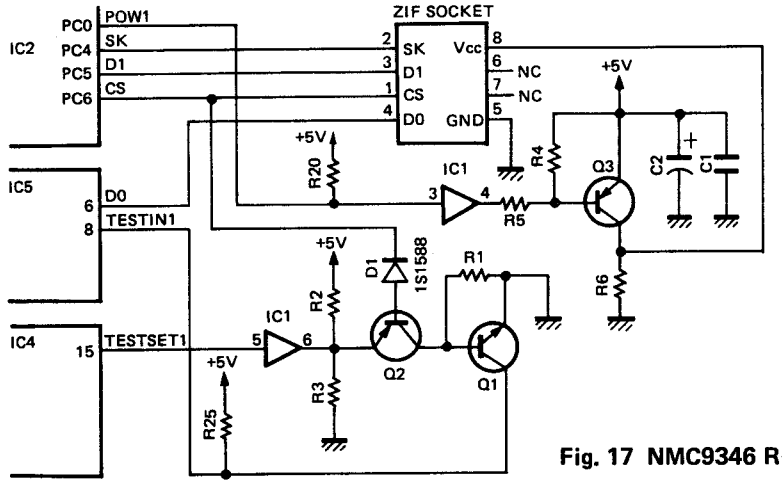


Fig. 17 NMC9346 ROM Write Circuit Block Diagram

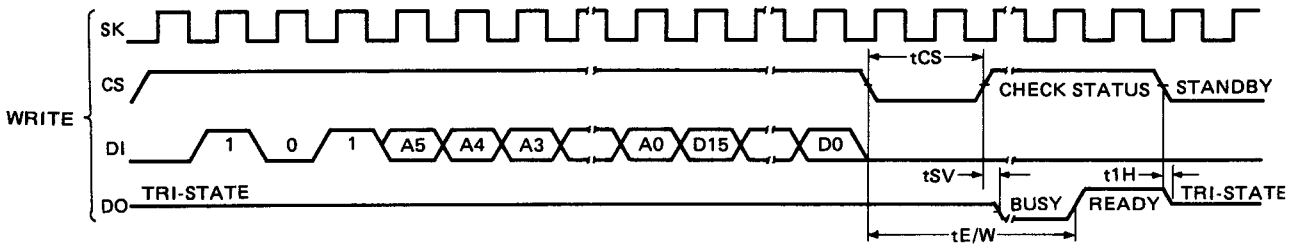


Fig. 18 NMC9346 ROM Write Timing Chart

LCD Interface Circuit

The LCD interface circuit consists of direct connections of the data bus lines from the buffer in the CPU board unit and other control lines. R26 is used for adjusting the contrast of the LCD ass'y (B30-0304-08). A small resistance value gives a dark display; a high resistance value gives a light display.

Pin No.	Terminal name	I/O	Function
1	V_{DD} (+ 5V)	I	Power supply pin (5V±5%)
2	CSI	I	Chip select pin
3	ENB	I	Clock input pin
4	RD	I	Busy flag read input pin
5	WR	I	Data write input pin
6	A0	I	Switches character code or instruction input
7~14	D0~D7	I	Data input; D7 is an I/O pin
15	NC	I	Not connected
16	$\overline{RESET}$	I	Reset signal input pin
17	VOUT	I	Contrast adjustment control pin
18	V_{SS} (GND)	I	Power supply pin (0V)

Table 5 LCD Interface Circuit Pin Function

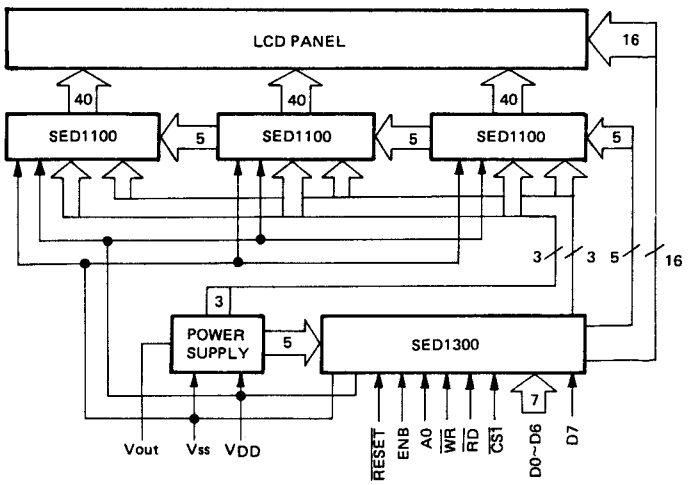
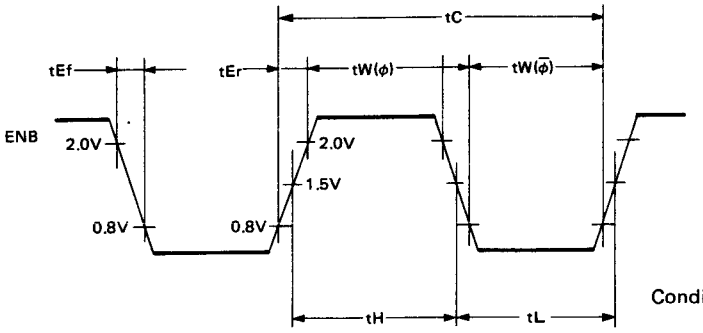


Fig. 19 LCD Interface Circuit Block Diagram

CIRCUIT DESCRIPTION

AC Characteristics (Timing Chart)

1. Clock Signals



Condition : V_{DD} = 5V±5%,
Top = 0~50°C

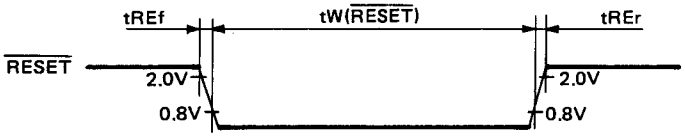
Fig. 20

Item	Symbol	Ratings			Units	Remarks
		Min	Typ	Max		
Enable clock period	tc	500	–	2000	ns	
Enable clock pulse width	tW (φ), tW (φ̄)	220	–	1050	ns	
Enable clock rise/fall time	tEr, tEl	–	–	50	ns	
Enable clock duty ratio	Duty	45	50	55	%	*1

Remarks *1 : Duty = t_H/ (t_H + t_L) x 100 (%)

Table 6

2. Reset Signals



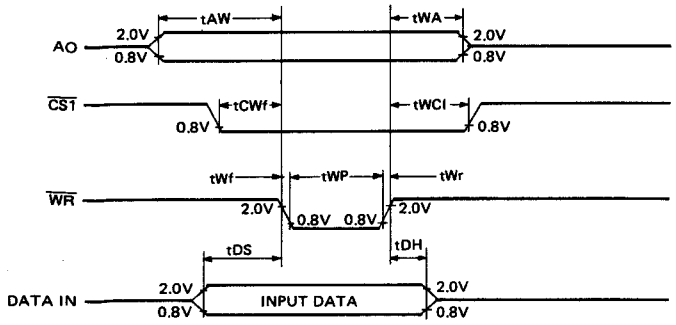
Condition : V_{DD} = 5V±5%, Top = 0~50°C

Fig. 21

Item	Symbol	Ratings			Units
		Min	Typ	Max	
Reset pulse width	tW (RESET)	5	–	–	ms
Reset pulse rise/fall times	tREf, tREr	–	–	500	μs

Table 7

3. Write Timing



Condition : V_{DD} = 5V±5%, Top = 0~50°C

Fig. 22

Item	Symbol	Ratings			Units
		Min	Typ	Max	
A0 → WR setup time	tAW	0	–	-	ns
CS1 → WR setup time	tCW1	0	–	-	ns
Write pulse width	tWP	350	–	tc ‹ 25	ns
Write pulse rise/fall time	tWr, tWf	–	–	50	ns
Data setup time	tDS	0	–	-	ns
A0 hold time	tWA	30	–	-	ns
CS1 hold time	tWC1	30	–	-	ns
Data hold time	tDH	30	–	-	ns

Table 8

CIRCUIT DESCRIPTION

Keyboard Interface Circuit

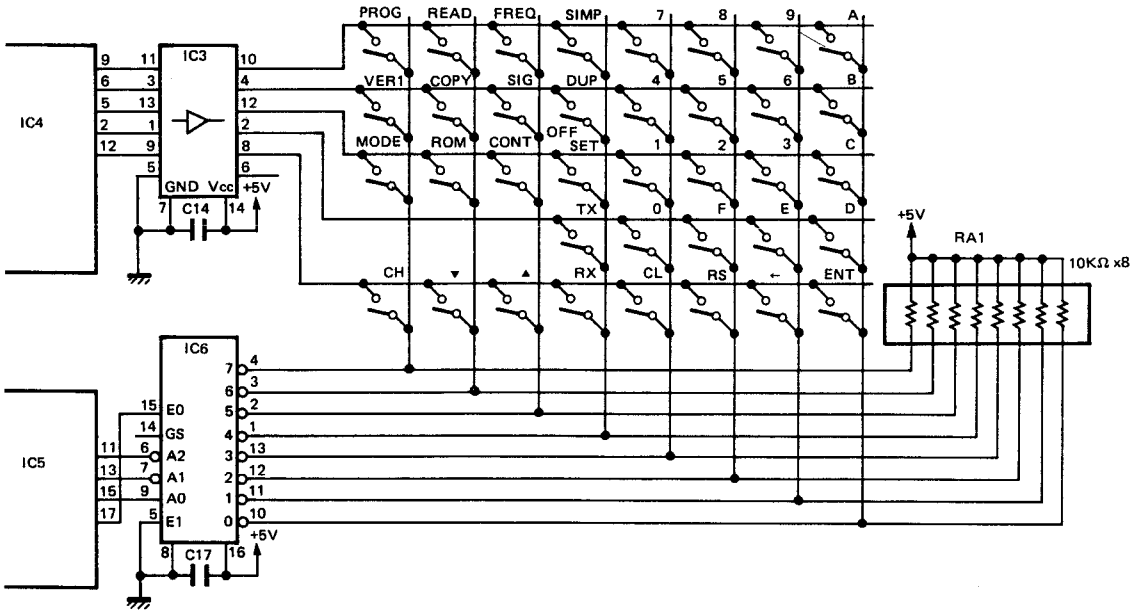


Fig. 23 Keyboard Interface Circuit Block Diagram

The keyboard interface circuit consists of IC3 and IC4 for the scan lines and IC5 and IC6 for the return lines, as shown in **Fig. 23**. To read the key codes, IC4 makes one bit at a time Low. If a key is pressed, the priority encoder (IC6) outputs a High signal at EO together with encoded signals from the return lines.

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	X	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Table 9 IC6 (Priority encoder)

CIRCUIT DESCRIPTION

Description of Components

CPU BOARD UNIT (W02-039X-08)

Components	Use/Function	Operation/Condition/Compatibility
IC1	External interface buffer	
IC2	RS-232C I/O	+ 5V → + 10V Transmit/receiver.
IC3	RS-232C I/O	+ 5V → + 10V Transmit/receiver.
IC4	External interface I/O	External interface I/O control.
IC5	RS-232C interface LSI	
IC6	Swithing regulator	+ 5V → + 21V 2764 ROM write power supply.
IC8	RAM	Working memory for microprocessor.
IC9	Keyboard unit interface buffer	Bus buffer.
IC10	OR	Memory and I/O control.
IC11	OR	Memory and I/O control.
IC12	Decoder	I/O address decoder.
IC14	RAM	Working memory for microprocessor.
IC15	Keyboard unit interface buffer	Bus buffer.
IC16	Reset circuit	Resets the microprocessor and I/O.
IC17	Schmitt inverter	Reset signal waveshaper.
IC18	Decoder	Memory address decoder.
IC20	EPROM	Program ROM (27256).
IC21	Keyboard unit interface buffer	Bus buffer.
IC22	Divider (1/2, 1/4)	4.9152MHz → 1/2, 1/4.
IC23	Inverter	
IC24	CTC	Internal timer, baud rate generator.
IC25	Microprocessor	8-bit microprocessor.
IC26	Three-pin regulator	+ 5V power supply for ICs.
Q1	Current booster	+ 5V supply current booster.
Q2	Current booster	+ 5V supply current booster.

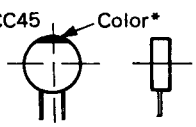
KEYBOARD UNIT (W02-0397-08)

Components	Use/Function	Operation/Condition/Compatibility
IC1	High-voltage buffer	Open-collector; protects I/O ports.
IC2	Three 8-bit parallel I/O ports	ROM write control.
IC3	High-voltage buffer	Open-collector buffer for keyboard scan lines.
IC4	I/O port	I/O for keyboard scan line.
IC5	I/O port	I/O for keyboard return.
IC6	Priority encoder	Keyboard return line encoder.
IC7	I/O port	ROM write control.
Q1	NMC9346 reverse insertion detector	
Q2	NMC9346 reverse insertion detector	
Q3	9346 Vcc switching	
Q4	2764 Vcc switching	
Q5	Power supply switching for reverse insertion detector	
Q6	2764 reverse insertion detector output	
Q7	Vpp + 21V switching	
Q8	Vpp + 5V switching	
D1	Q2 protection diode	
D2	Reverse current protector	
D3	+ 21V reverse current protector	

PARTS LIST

CAPACITORS CC 45 TH 1H 220 J
1 2 3 4 5 6

1 = Type ..... ceramic, electrolytic, etc.
2 = Shape .....round, square, etc.
3 = Temp. coefficient
4 = Voltage rating
5 = Value
6 = Tolerance



- **Capacitor value**

1 0 3 = 0.01μF
2 2 0 = 22pF
1st number | Multiplier
2nd number

0 1 0 = 1pF
1 0 0 = 10pF
1 0 1 = 100pF
1 0 2 = 1000pF = 0.001μF

- **Temperature Coefficient**

1st Word	C	L	P	R	S	T	U
Color*	Black	Red	Orange	Yellow	Green	Blue	Violet
ppm/°C	0	−80	−150	−220	−330	−470	−750

2nd Word	G	H	J	K	L
ppm/°C	± 30	± 60	± 120	± 250	± 500

Example CC45TH = −470±60 ppm/°C

- **Tolerance**

Code	C	D	G	J	K	M	X	Z	P	No code
(%)	± 0.25	± 0.5	± 2	± 5	± 10	± 20	+40 −20	+80 −20	+100 −0	More than 10μF−10~+50 Less than 4.7μF−10~+75

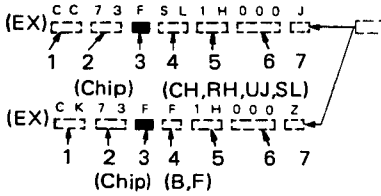
Code	B	C	D	F	G
(pF)	± 0.1	± 0.25	± 0.5	± 1	± 2

Less than 10 pF

- **Rating voltage**

2nd word / 1st word	A	B	C	D	E	F	G	H	J	K	V
0	1.0	1.25	1.6	2.0	2.5	3.15	4.0	5.0	6.3	8.0	–
1	10	12.5	16	20	25	31.5	40	50	63	80	35
2	100	125	160	200	250	315	400	500	630	800	–
3	1000	1250	1600	2000	2500	3150	4000	5000	6300	8000	–

- **Chip capacitors**

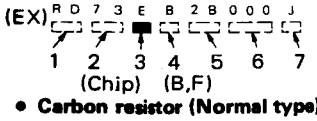


Dimension

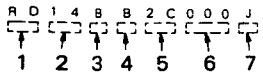
Dimension code	L	W	T
Empty	5.6 ± 0.5	5.0 ± 0.5	Less than 2.0
E	3.2 ± 0.2	1.6 ± 0.2	Less than 1.25
F	2.0 ± 0.3	1.25 ± 0.2	Less than 1.25

RESISTORS

- **Chip resistor (Carbon)**



- **Carbon resistor (Normal type)**



1 = Type ..... ceramic, electrolytic, etc.
2 = Shape ..... round, square, etc.
3 = Dimension
4 = Temp. coefficient
5 = Voltage rating
6 = Value
7 = Tolerance.

Dimension

Dimension code	L	W	T	Wattage
E	3.2 ± 0.2	1.6 ± 0.2	0.57	2B
F	2.0 ± 0.3	1.25 ± 0.2	0.45	2A

Rating wattage

Cord	Wattage	Cord	Wattage	Cord	Wattage
2A	1 /10W	2E	1/ 4W	3A	1W
2B	1/ 8W	2H	1/ 2W	3D	2W
2C	1/ 6W				

Dimension

PARTS LIST

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			KPT-20			
1	1A	*	A01-1036-08	CASE		
2	3A	*	A10-1287-08	CHASSIS		
3	1A	*	A21-1511-08	DRESSING PANEL		
4	1B	*	B10-0697-08	FRONT GLASS		
5	1B	*	B38-0304-08	LCD ASSY		
6	3B		B42-1745-04	SERIAL NO. PLATE		
7	1D		B46-0409-10	WARRANTY CARD	K,K2	
8	1D	*	B50-8168-00	INSTRUCTION MANUAL		
9	1A	*	E02-2005-08	ZIF SOCKET (28 PIN)		
10	1A	*	E02-2006-08	ZIF SOCKET (14 PIN)		
11	2B	*	E30-2086-08	RELAY CABLE		
12	2B	*	E30-2087-08	RELAY CABLE		
13	1B		E30-2078-05	DC POWER CORD		
14	2B	*	E31-3250-08	LEAD WITH CONNECTOR		
15	3A	*	E31-3252-08	LEAD WITH CONNECTOR		
17	3B	*	F19-0653-08	INSULATING PLATE	K,M	
18	3D	*	H01-8108-08	ITEM CARTON CASE		
19	1C	*	H12-1400-08	POLYSTYRENE FOAMED FIXTURE (UP)		
20	2C	*	H12-1401-08	POLYSTYRENE FOAMED FIXTURE (LOW)		
21	2D		H25-0060-03	PROTECTION BAG		
22	1C		H25-0104-04	PROTECTION BAG		
23	3A,3B	*	J02-0446-08	FOOT		
24	1A,2A	*	J31-0529-08	COLLAR		
A	2A		N10-2026-46	HEXAGON NUT		
B	2A		N10-2030-46	HEXAGON NUT		
C	2A		N15-1030-41	WASHER		
D	1B		N15-1030-46	WASHER		
E	2A,1B		N16-0030-46	SPRING WASHER		
F	1B		N30-3006-41	BINDING HEAD MACHINE SCREW		
G	3A	*	N35-2612-41	BINDING HEAD MACHINE SCREW		
H	2A		N35-3005-41	BINDING HEAD MACHINE SCREW		
J	3A,3B		N35-3006-45	BINDING HEAD MACHINE SCREW		
K	2B,3B		N35-3008-41	BINDING HEAD MACHINE SCREW		
S1	3A	*	S36-1411-08	SEESAW SWITCH		
			CPU BOARD UNIT (W02-039X-08)		**0396-08 : K,M 0398-08 : K**	
C1			C91-1020-05	CERAMIC 0.1μF 50WV		
C2		*	CE02W1V102M	ELECTRO 1000μF 35WV		
C3			CE02W1C101M	ELECTRO 100μF 16WV		
C4			CC45CH1H101J	CERAMIC 100PF J		
C5		*	CE02W1C102M	ELECTRO 1000μF 16WV		

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C7		*	CE02W1C102M	ELECTRO 1000μF 16WV		
C8–11		*	CE02W1E220M	ELECTRO 22μF 25WV	K2	
C12,13		*	CE02W1C470M	ELECTRO 47μF 16WV	K2	
C14			CC45SL1H220J	CERAMIC 22PF J		
C15		*	CE02W1E100M	ELECTRO 10μF 25WV		
C16–40			C91-1020-05	CERAMIC 0.1μF 50WV		
–		*	E02-2007-05	IC SOCKET (8 PIN)		
–			E02-2001-05	IC SOCKET (28 PIN)		
J1		*	E08-5071-08	SQUARE SOCKET		
J2		*	E40-7202-05	CONNECTOR		
J3		*	E03-0167-08	DC JACK CONNECTOR		
J4		*	E06-0755-08	DIN JACK		
J5		*	E08-2573-05	CONNECTOR		
L1		*	L39-0429-08	COIL (250μH)		
X1		*	L77-1341-08	CRYSTAL RESONATOR (4.9152MHZ)		
R1		*	RD14BB2H1R0J	RD 1.0 J 1/2W		
R2			RS14DB3A101J	FL-PROOF RS 100 J 1W		
R3,4		*	RW98A3H0R5J	CEMENT 0.5 J 5W		
R5		*	RS14DB2E203J	FL-PROOF RS 20K J 1/4W		
R6		*	RS14DB2E122J	FL-PROOF RS 1.2K J 1/4W		
R7–9			RD14BB2C103J	RD 10K J 1/6W		
R10			RD14BB2C470J	RD 47 J 1/6W		
R11			RD14BB2C103J	RD 10K J 1/6W		
R12			RD14BB2C221J	RD 220 J 1/6W		
R13			RD14BB2C561J	RD 560 J 1/6W		
R14			RD14BB2C221J	RD 220 J 1/6W		
R15			RD14BB2C182J	RD 1.8K J 1/6W		
R16			RD14BB2C103J	RD 10K J 1/6W		
D1			U15B	DIODE		
IC1			SN74LS244N	IC (EXT. I/F BUFF.)		
IC2,3		*	MAX232	IC (RS-232C I/O)	K2	
IC4		*	SN74LS273N	IC (EXT. I/F I/O)		
IC5		*	μPD8251AP-5	IC (RS-232C I/F LSI)	K2	
IC6			TL497ACN	IC (SWITCHING REGULATOR)		
IC8		*	MB8464-15L	IC (RAM)		
IC9			SN74LS244N	IC (KEYBOARD UNIT I/F BUFF.)		
IC10,11			SN74LS32N	IC (OR X2)		
IC12			SN74LS139N	IC (DECODER)		
IC14		*	MB8464-15L	IC (RAM)		
IC15			SN74LS244N	IC (KEYBOARD UNIT I/F BUFF.)		

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IC16			PST520C	IC (RESET IC)		
IC17		*	SN74LS14	IC (SCHMITT INVERTER)		
IC18			SN74LS139N	IC (DECODER)		
IC20		*	MBM27256	IC (EPROM)		
IC21			SN74LS245N	IC (KEYBOARD UNIT I/F BUFF.)		
IC22			SN74LS74N	IC (DIVIDER 1/2, 1/4)		
IC23			SN74LS04N	IC (INVERTER)		
IC24		*	LH0082A	IC (CTC)		
IC25			LH0080A	IC (MICROPROCESSOR)		
IC26			L7805	IC (THREE-PIN REGULATOR)		
Q1,2		*	2SA1265R	TRANSISTOR		
KEYBOARD UNIT (W02-0397-08)						
C1			C91-1020-05	CERAMIC 0.1μF 50WV		
C2,3		*	CE02W1C100M	ELECTRO 10μF 16WV		
C4,5			C91-1020-05	CERAMIC 0.1μF 50WV		
C6		*	CE02W1H100M	ELECTRO 10μF 50WV		
C7			C91-1020-05	CERAMIC 0.1μF 50WV		
C8		*	CE02W1C100M	ELECTRO 10μF 16WV		
C9		*	CE02W1H1R0M	ELECTRO 1.0μF 50WV		
C10–17			C91-1020-05	CERAMIC 0.1μF 50WV		
S1		*	E02-2003-08	IC SOCKET (14 PIN)		
S2		*	E02-2004-08	IC SOCKET (28 PIN)		
—		*	E31-3251-08	LEAD WITH CONNECTOR		
J2		*	E40-5104-08	PIN ASSY		
S3–39		*	S40-1413-08	TACT SWITCH		
R1			RD14BB2E102J	RD 1K J 1/4W		
R2			RD14BB2E122J	RD 1.2K J 1/4W		
R3			RD14BB2E102J	RD 1K J 1/4W		
R4–7			RD14BB2E103J	RD 10K J 1/4W		
R8			RD14BB2E511J	RD 510 J 1/4W		
R9			RD14BB2E202J	RD 2K J 1/4W		
R10			RD14BB2E512J	RD 5.1K J 1/4W		
R11			RD14BB2E100J	RD 10 J 1/4W		
R13			RD14BB2E222J	RD 2.2K J 1/4W		
R14,15			RD14BB2E102J	RD 1K J 1/4W		
R16–18			RD14BB2E202J	RD 2K J 1/4W		
R19–24			RD14BB2E103J	RD 10K J 1/4W		
R25			RD14BB2E102J	RD 1K J 1/4W		
R26			RD14BB2E153J	RD 15K J 1/4W		
R27			RD14BB2E512J	RD 5.1K J 1/4W		
R28			RD14BB2E561J	RD 560 J 1/4W		
R29		*	RD14BB2E361J	RD 360 J 1/4W		

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
RA1,2			R90-0229-05	RESISTOR BLOCK (10KΩ X 8)		
D1,2			1S1588	DIODE		
D3		*	SIS3M	DIODE		
IC1		*	SN74LS07	IC (HIGH-VOLTAGE BUFF.)		
IC2			μPD8255AC-5	IC (THREE 8-BIT PARALLEL I/O PORTS)		
IC3		*	SN74LS07	IC (HIGH-VOLTAGE BUFF.)		
IC4		*	SN74LS273N	IC (I/O PORT)		
IC5			SN74LS244N	IC (I/O PORT)		
IC6		*	SN74LS148	IC (PRIORITY ENCODER)		
IC7		*	SN74LS273N	IC (I/O PORT)		
Q1			2SC1815GR	TRANSISTOR		
Q2–5			2SA1015Y	TRANSISTOR		
Q6			2SC1815GR	TRANSISTOR		
Q7,8			2SA1015Y	TRANSISTOR		
Q9			2SA1815GR	TRANSISTOR		

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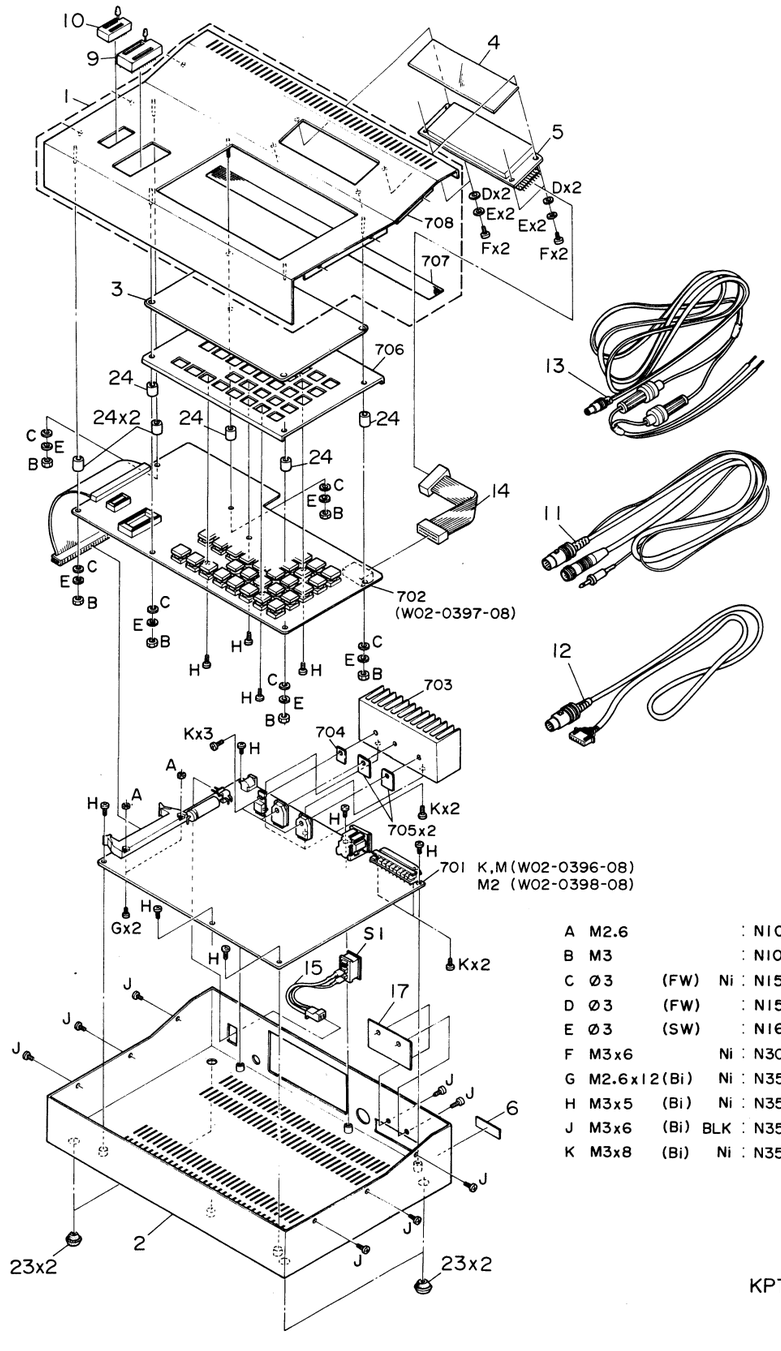
EXPLODED VIEW

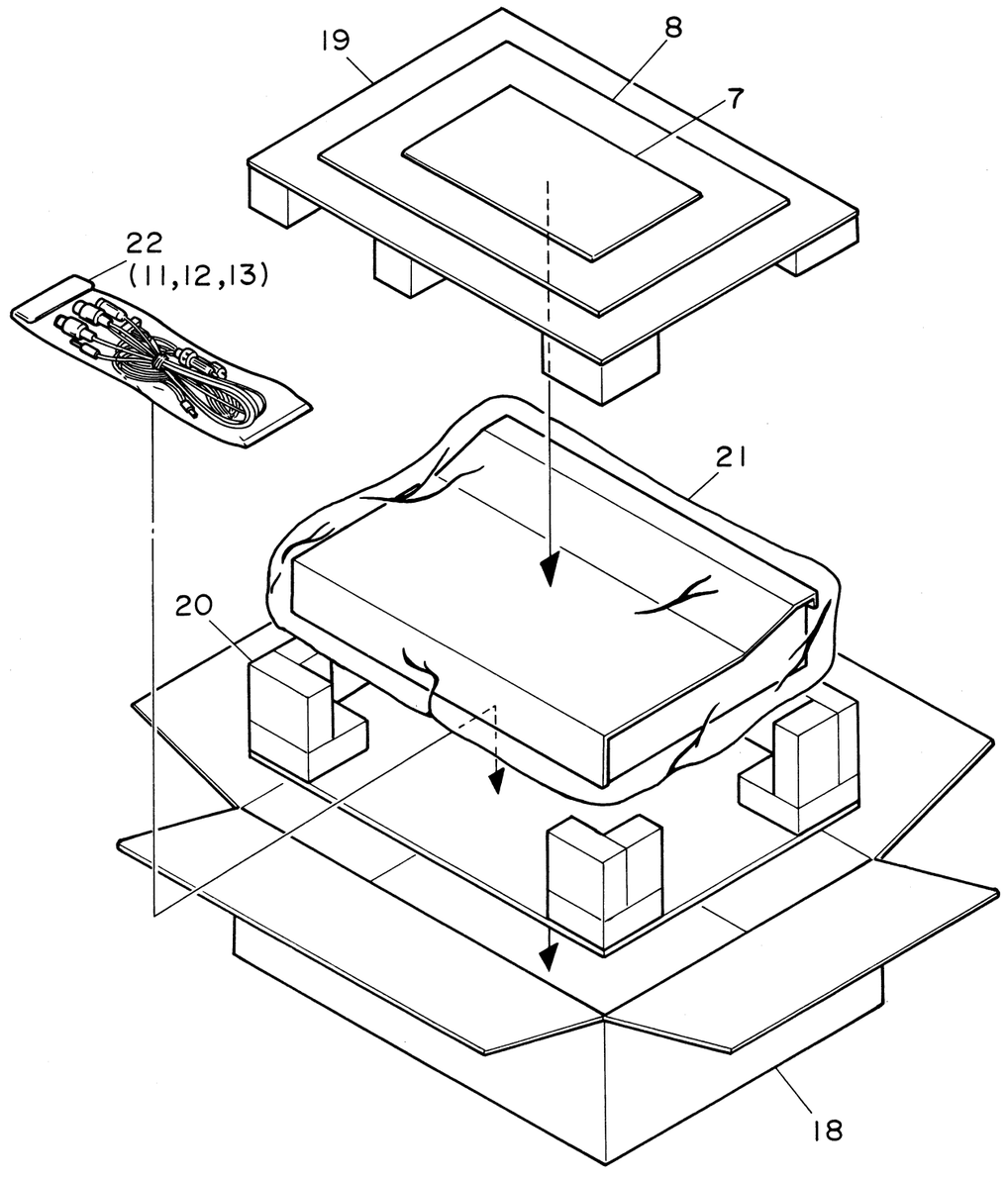


A	M2.6			: N10-2026-46
B	M3			: N10-2030-46
C	Ø3	(FW)	Ni	: N15-1030-41
D	Ø3	(FW)		: N15-1030-46
E	Ø3	(SW)		: N16-0030-46
F	M3x6		Ni	: N30-3006-41
G	M2.6x12	(Bi)	Ni	: N35-2612-41
H	M3x5	(Bi)	Ni	: N35-3005-41
J	M3x6	(Bi)	BLK	: N35-3006-45
K	M3x8	(Bi)	Ni	: N35-3008-41

KPT-20

Parts with the exploded numbers larger than 700 are not supplied.

PACKING



KPT-20

Parts with the exploded numbera larger than 700 are not supplied.

SCHEMATIC

IC1,9,15 : SN74LS244N
IC2,3 : MAX232
IC4 : SN74LS273N
IC5 : μPD8251AP-5
IC6 : TL497ACN
IC8,14 : MB8464-15L
IC10,11 : SN74LS32N
IC12,18 : SN74LS139N
IC16 : PST520C
IC17 : SN74LS14
IC20 : MBM27256
IC21 : SN74LS245N
IC22 : SN74LS74N
IC23 : SN74LS04N
IC24 : LH0082A
IC25 : LH0080A
IC26 : L7805
Q1, 2 : 2SA1265R
D1 : U15B

DESTINATION \ REF NO.	IC2,3,5	C8~13,19	J5
W02-0396-08 (K) (M)	NO	NO	NO
W02-0398-08 (K2)	YES	YES	YES

CPU BOARD UNIT (W02-0396-08)

RS-232C I/F

*J5

TRANSMIT/RECEIVE

*IC5 USART

*IC3

*IC2

IC1

IC4

IC7

IC8

IC10 (1/5)

IC10 (2/5)

IC10 (3/5)

IC10 (4/5)

IC10 (5/5)

IC11 (4/5)

IC11 (1/5)

IC11 (3/5)

IC11 (2/5)

IC11 (5/5)

IC12

IC13

IC14

IC16

IC17 (1/7)

IC17 (2/7)

IC17 (3/7)

IC17 (4/7)

IC17 (5/7)

IC17 (6/7)

IC17 (7/7)

IC18

IC19

IC20

IC22 (1/3)

IC22 (2/3)

IC22 (3/3)

IC23 (1/7)

IC23 (2/7)

IC23 (3/7)

IC23 (4/7)

IC23 (5/7)

IC23 (6/7)

IC23 (7/7)

IC24

IC25

IC26

MEMORY ADDRESS CONTROL

I/O ADDRESS CONTROL

μ-PROCESSOR

RESET

POWER SW

S1

J2

J3 DC IN

D1

Q1

Q2

13.8V

5V

21V

EXT DI

CPU STP

EXT CS1

EXTSK

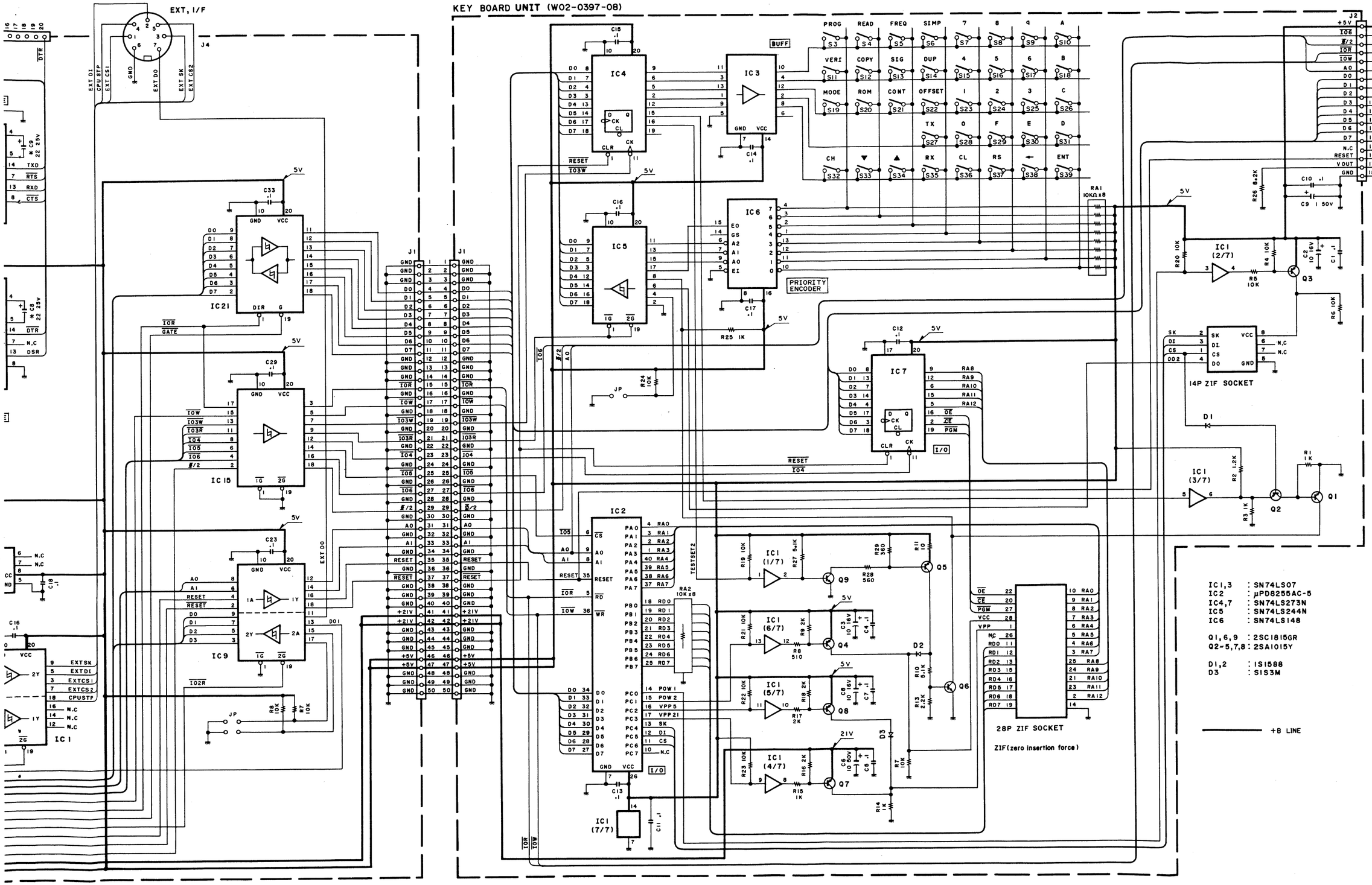
EXTDI

EXTCS1

EXTCS2

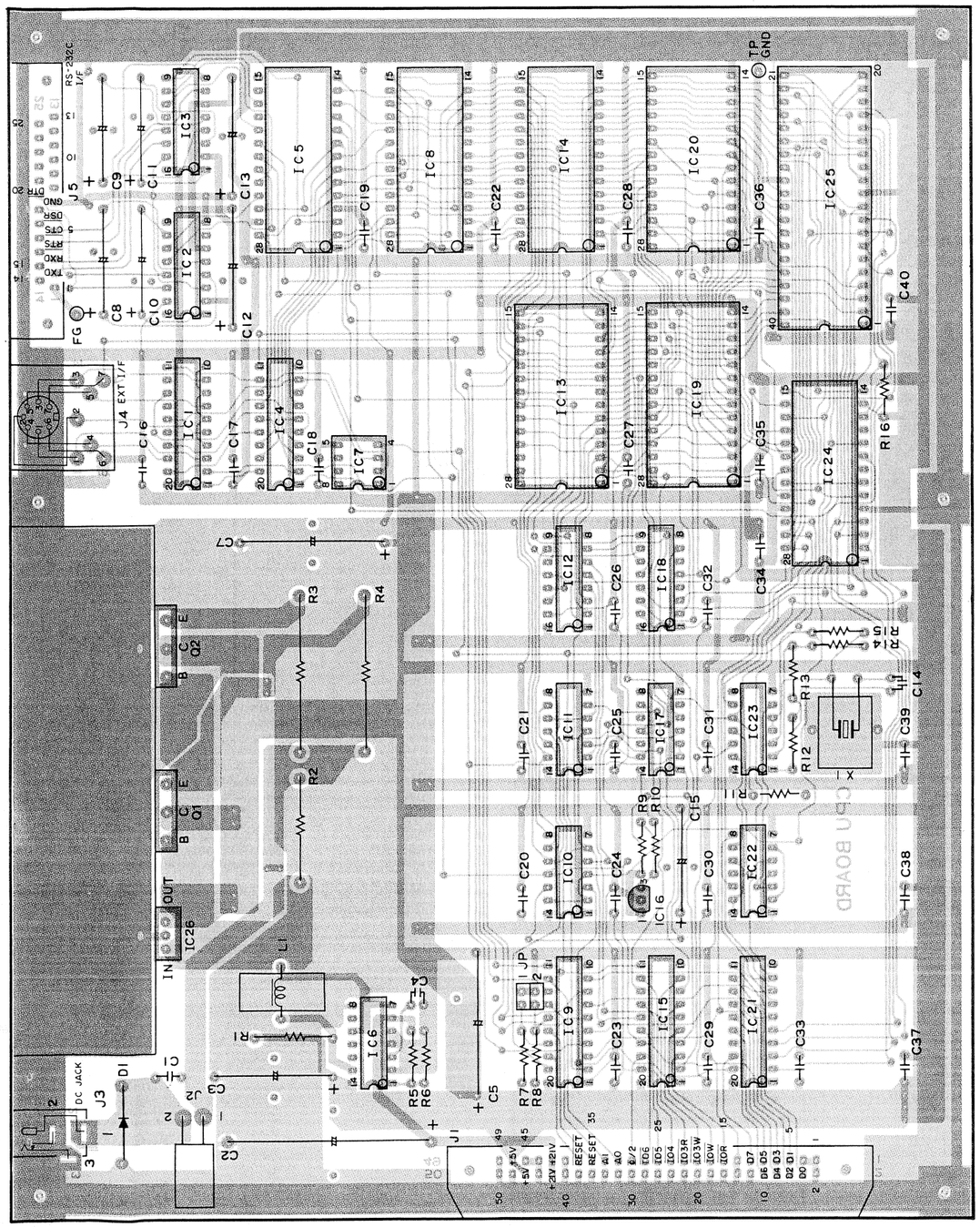
CPUSTP

HEMATIC DIAGRAM

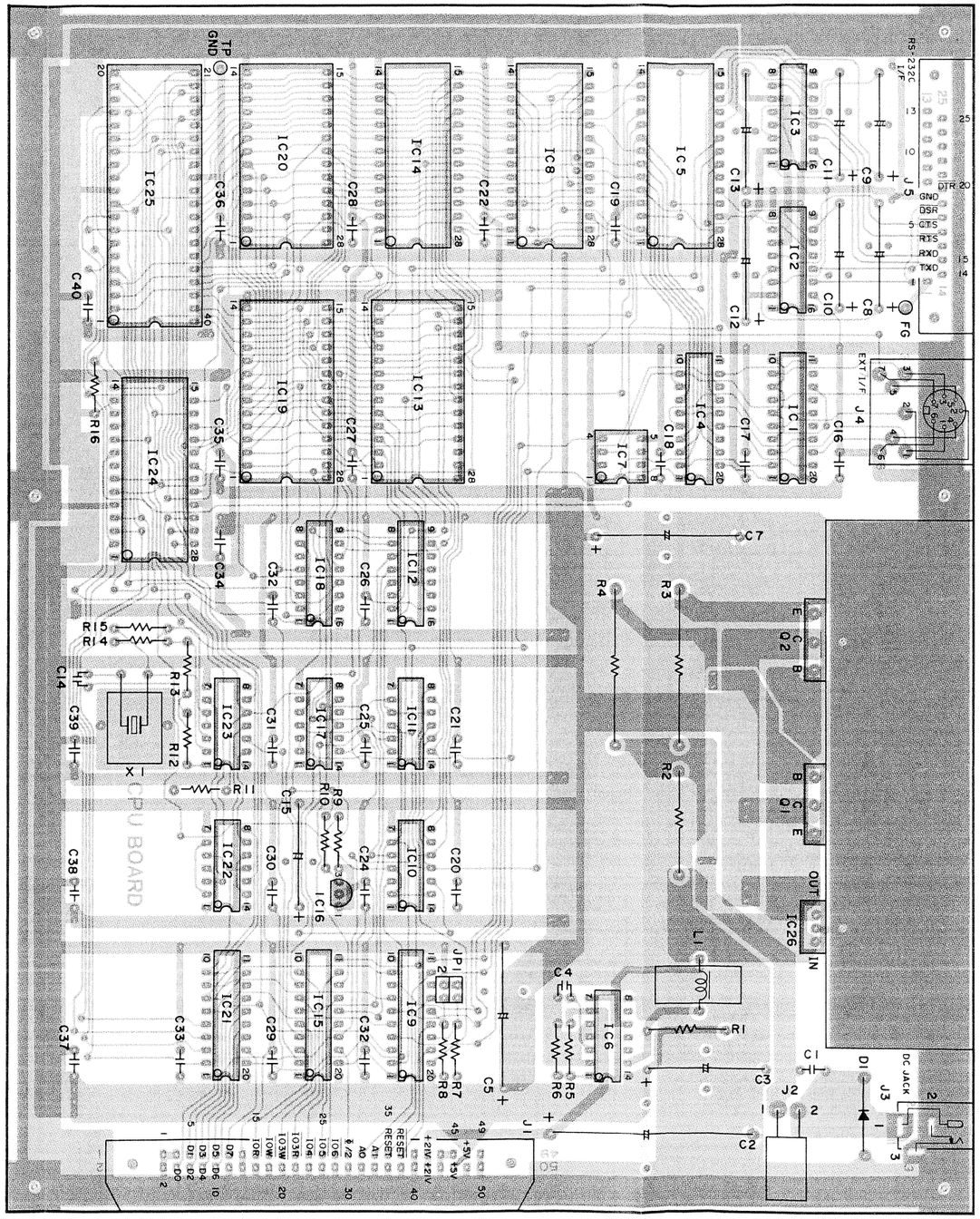


KPT-20 PC BOARD VIEWS

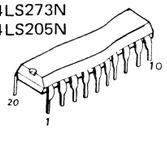
▼CPU BOARD UNIT (W02-039X-08) Component side view



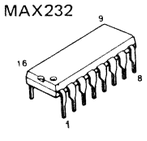
▼CPU BOARD UNIT (W02-039X-08) Foil side view



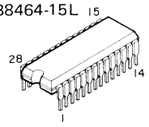
SN74LS244N
SN74LS273N
SN74LS205N



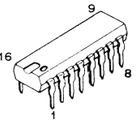
MAX232



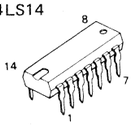
μPD8251AP-5
MB8464-15L



SN74LS139N

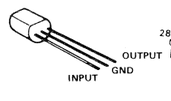


TL497ACN
SN74LS32N
SN74LS14



SN74LS74N
SN74LS04N

PST520C



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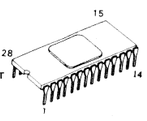
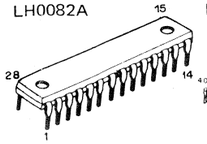


LH0082A



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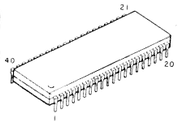
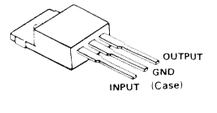


L7805



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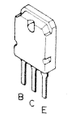
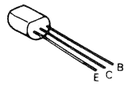
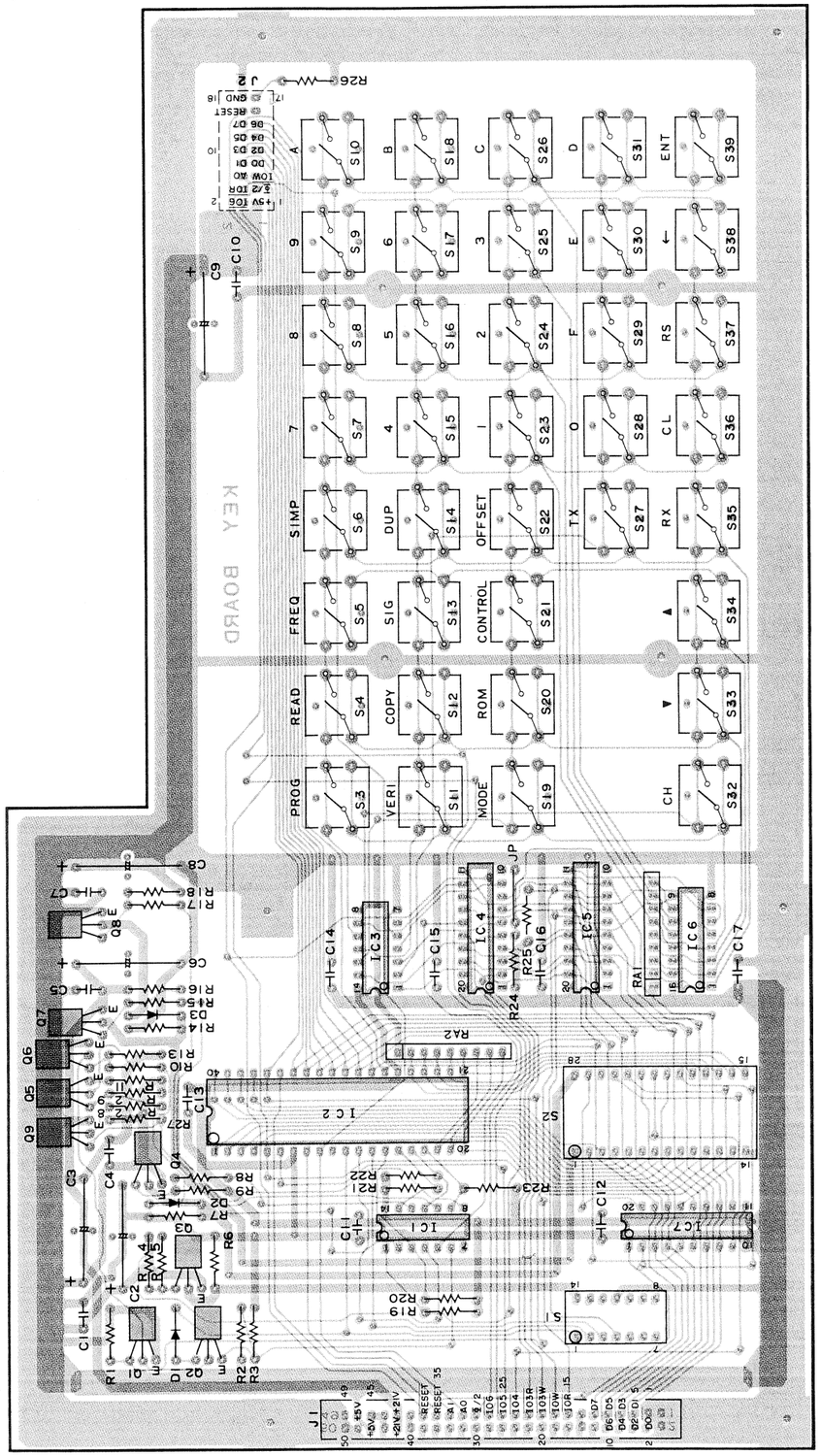


2SA1015Y
2SC1815GR

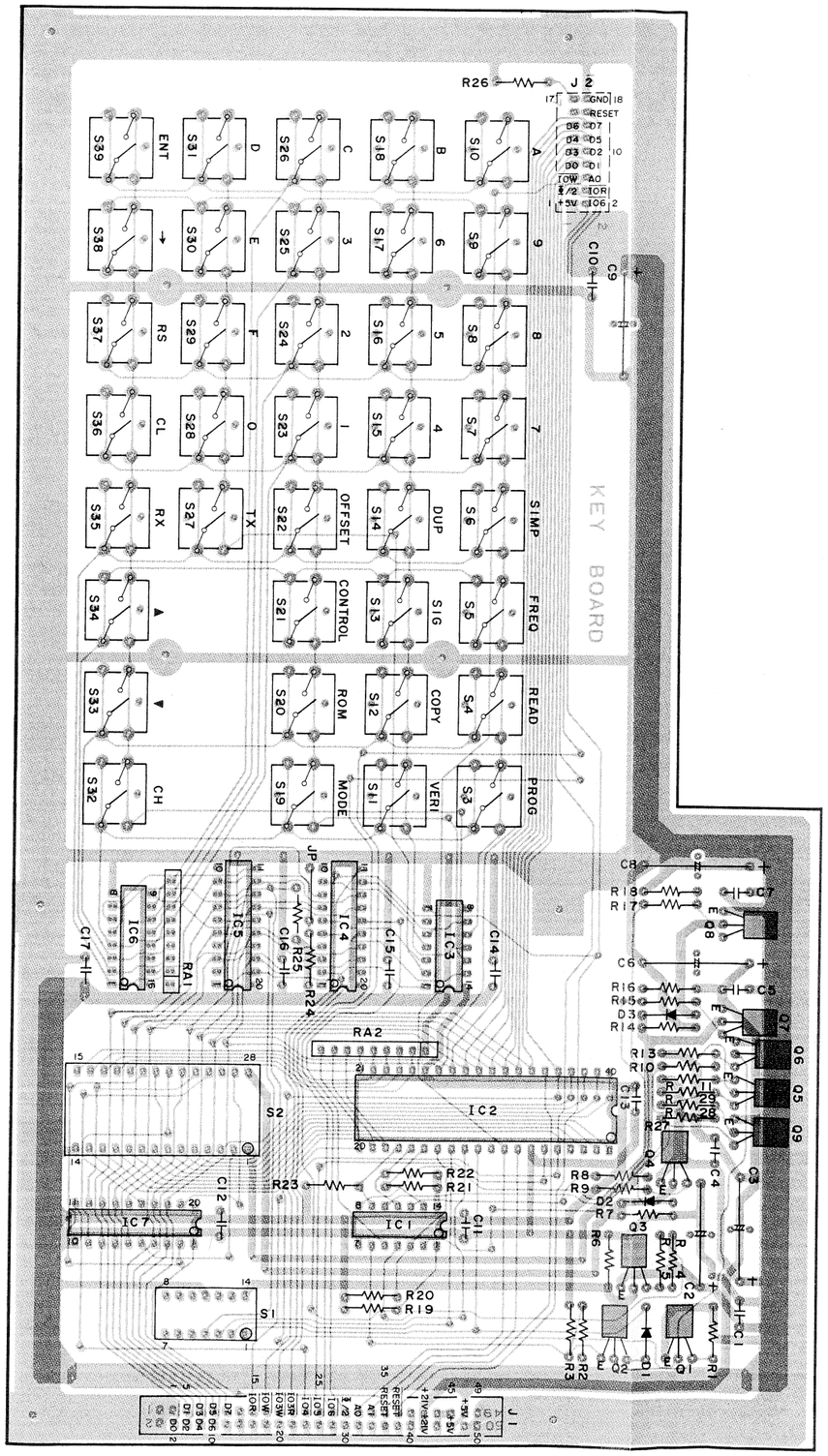


▼KEYBOARD UNIT (W02-0397-08) Component side view

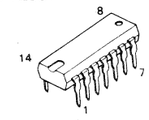


IC1 : SN74LS07 IC2 : μPD8255AC-5 IC3 : SN74LS07 IC4 : SN74LS273N IC5 : SN74LS273N IC6 : SN74LS148 IC7 : SN74LS273N
Q1 : 2SC1815GR Q2~5 : 2SA1015Y Q6 : 2SC1815GR Q7,8 : 2SA1015Y Q9 : 2SC1815GR

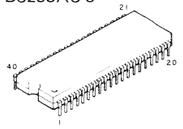
▼KEYBOARD UNIT (W02-0397-08) Foil side view



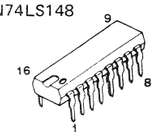
SN74LS07



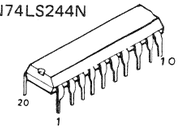
μPD8255AC-5



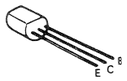
SN74LS148



SN74LS273N
SN74LS244N



2SA1015Y
2SC1815GR



KPT-20

SPECIFICATIONS

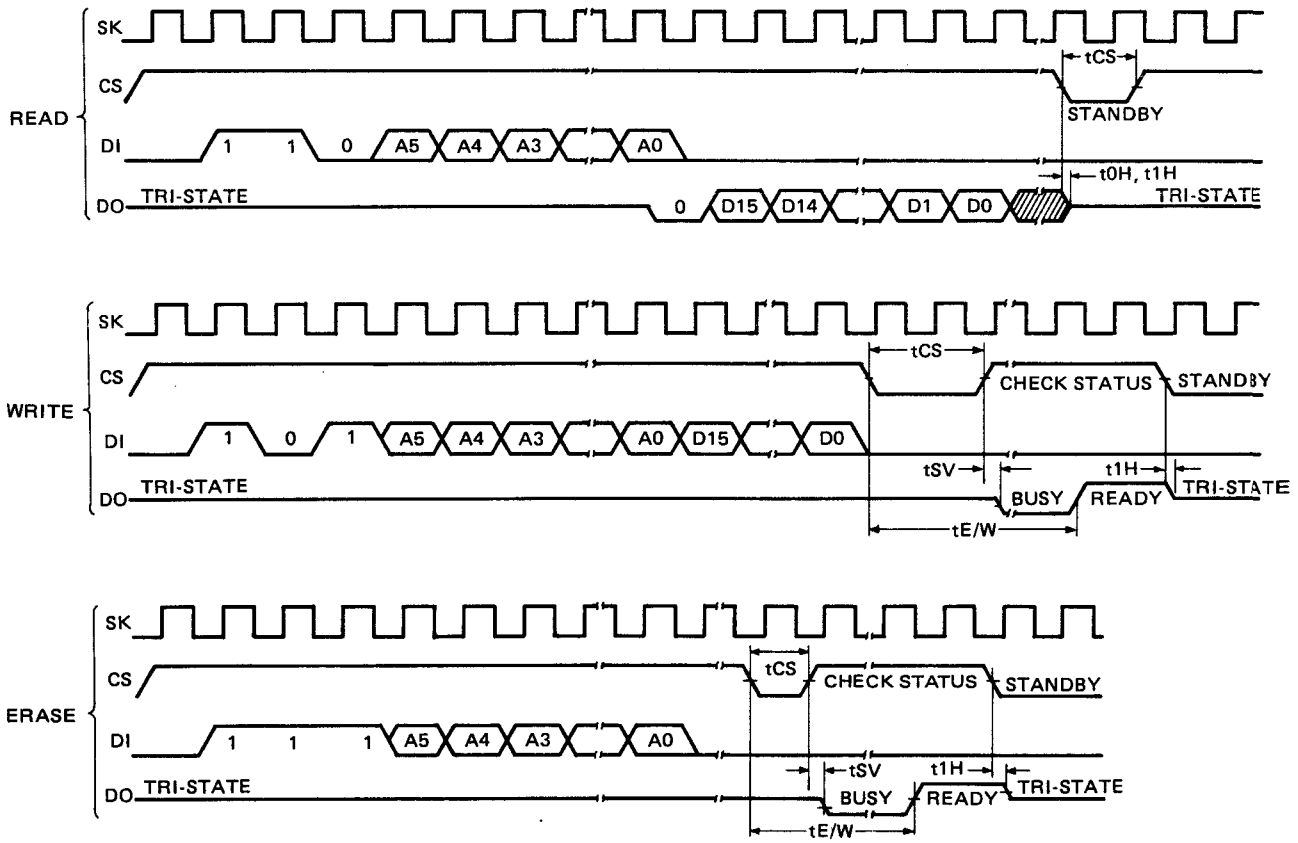
1) Frequency range :

UHF 400~512MHz (12.5kHz step)
VHF 150~174MHz (5kHz step)

2) Used EEPROM

NMC9346 (16-bit x 64W)

3) Timing diagram



4) Size

	Body	Package
H :	70mm	157mm
D :	215mm	262mm
W :	315mm	362mm

5) Weight

2.4kg (Body)
3.0kg (incl. option)

Design and specifications subject to change without notice.

KENWOOD CORPORATION
Shionogi Shibuya Building, 17-5, 2-chome Shibuya, Shibuya-ku, Tokyo 150, Japan

KENWOOD COMMUNICATIONS
Post Office Box 7065, Compton, California 90224, U.S.A.

KENWOOD COMMUNICATIONS
DIVISION OF KENWOOD ELECTRONICS, DEUTSCHLAND GMBH
Rembrücker Str. 15, 6056 Heusenstamm, West Germany

KENWOOD ELECTRONICS, BENELUX N.V.
Mechelsesteenweg 418 B-1930 Zaventem, Belgium

KENWOOD ELECTRONICS, AUSTRALIA PTY. LTD.
4E. Woodcock Place, Lane Cove, N.S.W. 2066, Australia